IN THE SPECIFICATION

Please amend the paragraph that starts at page 1, line 32 as follows:

One of the problems that needed to be solved was how to signal the transceivers at each end of the bus that reset processing (the so-called OOB signalling interval -- OOB standing for Out Of Band) needed to start when anything went wrong with the transfers of data over the bus such as loss of synchronization. The OOB interval is an interval on the bus when processing is performed to calibrate the bus, achieve synchronization and do other things that are not relevant to the invention. The invention described herein only has to do with circuitry used transmit an OOB signal to indicate the need for OOB processing and for recognition of the OOB signal.

Please amend the paragraph that starts at page 2, line 33 as follows:

The assignee of the invention devised an OOB signal and protocol. This innovation was adopted by the group developing the serial ATA bus standard and is described in a U.S. patent application entitled **SIGNALLING PROTOCOL FOR SIGNALLING START OF RESET PROCESSING IN SERIAL ATA BUS PROTOCOL,** filed 02/01/2002, serial number 10/061,883 which is hereby incorporated by reference. This signalling process is referred to in the serial ATA bus standard as part of the OOB protocol.

Please amend the paragraph starting at page 10, line 24 as follows:

Detection of an OOB signal using conventional Fiber Channel receivers involves monitoring the data content of a serial-in, parallel-out register 50 coupled to the output of a conventional Fiber Channel receiver 52 and processing the data therein to recognize an OOB pattern. The pattern recognition circuitry is all the circuitry in Figure 5 other than the receiver 52 and the shift register 50. This

pattern recognition circuitry monitors the data in output register 50 at all times when the bus is active and at all time when the bus is in sleep mode. To do this however, the high power receiver 52 can never go to sleep when the bus 56 ~~52~~ and 54 is in sleep mode. In alternative embodiments, the pattern recognition circuitry is coupled directly to the input lines 54 and 56 and is modified to detect common mode voltage conditions on lines 54 and 56 and time them and then to compare the duration of each common mode interval and the pattern of common mode intervals to a predetermined pattern of common mode intervals that define the OOB signal. Such a circuit is shown in Figure 6.

Please amend the paragraph which starts at page 14, line 9 as follows:

Figure 6 is a block diagram of a OOB receiver using a conventional high power Fiber Channel receiver which can go into sleep mode and power down and having low power OOB pattern recognition circuitry coupled to the input of the receiver. A conventional Fiber Channel or other receiver 51 monitors the bus 54 and 56 and receives high speed data transmitted thereon. Contrary to receiver 52 in Figure 5, receiver 51 is of a type which can power down in sleep mode. The bus 54 ~~55~~ and 56 can be differential mode or a singled ended bus in which case receiver 51 is singled ended. The invention is applicable to any serial format data bus wherein data or fill data needs to be transmitted at all times and wherein there is a need to send a reset signal when synchronization is lost or when the bus needs to be awakened from sleep.